Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (currently amended) A method for forming a dual damascene structure, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer of a first thickness over said silicon substrate;

forming a first etch stop layer over said first dielectric layer;

forming a second dielectric layer of a second thickness over said first dielectric layer;

forming an anti-reflective coating layer over said second dielectric layer prior to etching of a first trench;

etching said first trench in said second dielectric layer; ~~and~~

simultaneously etching a second trench to a first depth in said second dielectric layer and etching said first trench in said first dielectric layer wherein the first depth is approximately equal to the second thickness; ~~.~~

removing the first etch stop layer at a bottom portion of the first trench;

forming a liner film in the first trench and the second trench; and

forming a contiguous copper layer in the first trench and the second trench.

2. (original) The method of claim 1 wherein said anti-reflective coating layer comprises silicon oxynitride.

3. (previously presented) The method of claim 1 wherein first etch stop layer is formed with material selected from the group consisting of silicon carbide and silicon nitride.

4. (currently amended) The method of claim 1 wherein said first dielectric layer is OSG ~~FSG~~.

5. (currently amended) The method of claim 1 wherein said second dielectric layer is OSG ~~FSG~~.

6. (canceled)

7. (currently amended) A method for forming a copper filled dual damascene structure, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first dielectric layer of a first thickness over said silicon substrate;

forming a first etch stop layer over said first dielectric layer;

forming a second dielectric layer of a second thickness over said first dielectric layer;

forming a silicon oxynitride anti-reflective coating layer over said second dielectric layer prior to etching a first trench in said second dielectric layer;

etching said first trench to a first depth in said second dielectric layer and said first dielectric layer wherein the first depth is greater than the thickness of said second dielectric layer; ~~and~~

simultaneously etching a second trench to a second depth in said second dielectric layer and etching said first trench in said first dielectric layer wherein the second depth is approximately equal to the second thickness; ~~.~~

removing the first etch stop layer at a bottom portion of the first trench;

forming a liner film in the first trench and the second trench; and

forming a contiguous copper layer in the first trench and the second trench.

8. (previously presented) The method of claim 7 wherein said silicon nitride anti-reflective coating layer comprises 30 to 50 atomic percent of silicon, 20 to 50 atomic percent of oxygen, 2 to 17 atomic percent of nitrogen, and 7 to 35 atomic percent of hydrogen.

9. (previously presented) The method of claim 7 wherein first etch stop layer is formed with material selected from the group consisting of silicon carbide and silicon nitride.

10. (currently amended) The method of claim 7 wherein said first dielectric layer is OSG ~~FSG~~.

11. (currently amended) The method of claim 7 wherein said second dielectric layer is OSG ~~FSG~~.

12. (canceled)

13 -17. (canceled)

18. (previously presented) A method for forming a dual damascene structure, comprising:

providing a silicon substrate containing one or more electronic devices;

forming a first etch stop layer over the silicon substrate;

forming a first dielectric layer over the first etch stop layer;

forming a second etch stop layer over the first dielectric layer;

forming a second dielectric layer over the second etch stop layer;

forming an anti-reflective coating layer over the second dielectric layer prior to etching of a first trench;

etching the first trench having a first width through the anti-reflective coating layer, the second dielectric layer, and the second etch stop layer;

concurrently etching a second trench having a second width greater than the first width through the second dielectric layer down to the second etch stop layer and etching the first trench through the first dielectric layer down to the first etch stop layer, wherein the second trench overlies the first trench;

removing the first etch stop layer at a bottom portion of the first trench;

forming a liner film in the first trench and the second trench; and

forming a contiguous copper layer in the first trench and the second trench.

19. (canceled)

20. (canceled)